Design Strategy for a Piezoelectric Nanogenerator with a Well-Ordered Nanoshell Array

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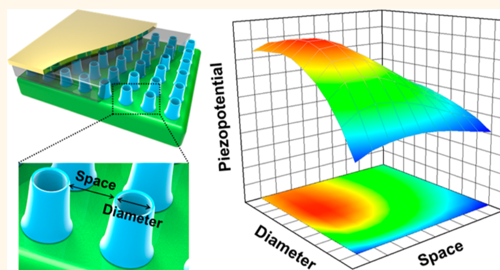
ABSTRACT The piezoelectric nanogenerator (PNG) has been spotlighted as a promising candidate for use as a sustainable power source in wireless system applications. For the further development of PNGs, structural optimization is essential, but the structural analysis progress in this area has been scant. In the present study, we proposed a PNG with a well-ordered nanoshell array structure. The nanoshell structure has been considered as an effective core nanostructure for PNGs due to its effective stress confinement effect but has not been experimentally introduced thus far due to the challenging fabrication method required. To produce a controllable nanoshell structure, a top-down silicon nanofabrication technique which involves advanced spacer lithography is introduced. A comprehensive design strategy to enhance the piezoelectric performance is proposed in terms of the nanoshell diameter and shell-to-shell space. Both simulated and measured data confirm that an extremely high density of a structure is not always the best answer to maximize the performance. The highest amount of power can be achieved when the shell diameter and shell-to-shell space are within their proper ranges. The structural design strategy studied in this work provides a guideline for the further structural developments of PNG.



KEYWORDS: piezoelectric nanogenerator · nanoshell · barium titanate · spacer lithography · energy harvesting

Piezoelectric energy harvesters have been widely investigated due to their known advantages over other mechanical energy harvesters. Above all, abundant energy sources and good scalability are the most important characteristics because these two issues are essential for implementation into wireless system applications. To enhance the performance and to increase the application area with the limited dimension, there have been many attempts at hybridization between a piezoelectric energy harvester and a nanostructure since 2006.[1] A mechanical energy harvester created with a nanoscale piezoelectric material is referred to as a piezoelectric nanogenerator (PNG). Mechanical movements such as bending,[2,3] vibration,[4] ultrasonic waves,[5,6] sound,[7,8] magnetic fields,[9] and cell expanding forces[10] have been successfully converted to electrical energy using various forms of PNGs. The performance levels of the PNGs are rapidly growing, and new applications are being intensively developed.

In spite of the rapid developments of PNGs, progress on structural evolution has been modest so far. The vertically grown nanowire bundle structure used at the prototype of PNG is still used in most devices.[1,5−7,11−13] The vertical nanowire bundle grown by bottom-up methods clearly has its own advantages, such as nanoscale dimension, high-throughput, and superior edge crystallinity. However, for the further evolution of PNG, effects of other advanced nanostructures and the comprehensive analyses on the various structural parameters have to be studied. Concrete design guidelines about the nanostructure are essential in the viewpoints of the structural optimization. Herein, we introduce a PNG with a perfectly well-ordered nanoshell array structure by means of a top-down silicon nanofabrication technique. By utilizing the notable structural controllability of the top-down process, the effects of structural parameters can be accurately controlled.

The nanoshell structure introduced in this work has been expected to present better performance than conventional nanorod or nanowire types owing to the enhanced

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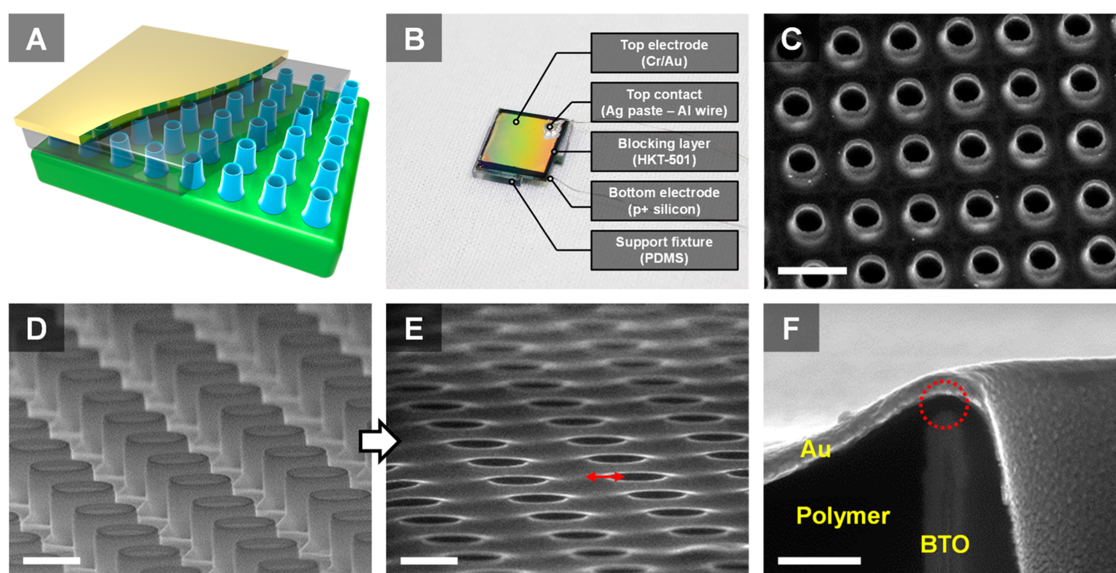

Figure 1. (A) Schematic describing the structure of the well-ordered nanoshell PNG. (B) Optical microscope image of the nanoshell PNG. (C) Top-view SEM image of the BTO nanoshell array. The scale bar is 5 μm. (D) Bird's-eye view SEM image of BTO nanoshell array. The scale bar is 2 μm. (E) Bird's-eye view SEM image of the final nanoshell PNG. The red arrow describes the cutting direction used in panel F. The scale bar is 2 μm. (F) Magnified side view of the final nanoshell PNG. The red dotted circle emphasizes the insulator margin. The scale bar is 500 nm.

stress confinement effect.[14] Stress applied along an axis can be more effectively confined due to the effect of the nanostructure, which results in the enhancement of the piezopotential. This confinement effect becomes stronger for thinner shell thickness. However, the PNG with the nanoshell structure has not been experimentally demonstrated yet because of challenging fabrication issues. Conventional photolithography may not directly define the nanoscale thickness of the nanoshell as long as an extremely thin shell thickness is demanded. To fabricate the nanoshell array, state-of-the-art spacer lithography is adopted in this work. The origin of "spacer" in spacer lithography arises from the spacer and vertically stands along the sidewalls of a gate in a conventional metal oxide semiconductor field effect transistor (MOSFET). This type of spacer is created by the deposition of a film on a pre-existing dummy with a sacrificial pattern, with etching then done to remove all of the film material from the horizontal surfaces, leaving only the material on the sidewalls. By removing this sacrificial pattern, only the spacers, serving as a structural or hardmask layer for the subsequent etching process, remain on both sidewalls. Here, it is noteworthy that the minimum feature size is determined not by the lithographic resolution but by the deposited film thickness, thus overcoming the lithographic limit. Spacer lithography can produce uniformly patterned nanoshell arrays with sub-10 nm thicknesses at the wafer scale.[15−18] With a nanoshell PNG generated by spacer lithography, the degree of geometric parameter dependency can be closely analyzed by means of the excellent structural controllability that stems from the advantages of the top-down process.

RESULTS AND DISCUSSION

Figure 1 presents a schematic and images of the fabricated nanoshell PNG. The nanoshell PNG device is composed of the bottom silicon electrode, the BTO nanoshell array on the substrate, the blocking layer covering the nanoshell array, and the Au electrode on top of the device (Figure 1A). An optical image of the completely fabricated device is shown in Figure 1B. The final device presents a rainbow-colored surface due to the well-ordered repeating morphology. An insulator margin of 1 mm was formed around the edges of the device to prevent electrical shorting between the electrodes. To remove the undesirable roughness caused by the bottom electrode contact, a PDMS support fixture was inserted at the bottom.

A top-view SEM image of the BTO nanoshell array is presented in Figure 1C. Excellent shell-to-shell uniformity with a well-ordered characteristic is verified. The wafer-scale uniformity can be confirmed given the top-down fabrication schemes. Each of the geometric parameters such as the shell diameter (D), shell-to-shell space (S), shell height (H), and shell thickness (T) can be controlled simply by fine-tuning the fabrication steps. The example nanoshells shown in the SEM images have the diameter of 2.0 μm, a shell-to-shell space of 2.3 μm, a shell height of 2.2 μm, and a shell thickness of 250 nm (Figure 1D). After the deposition of the blocking layer and the top electrode, the exposed surface was planarized and only deep holes remain (Figure 1E). The most important role of the blocking layer is to

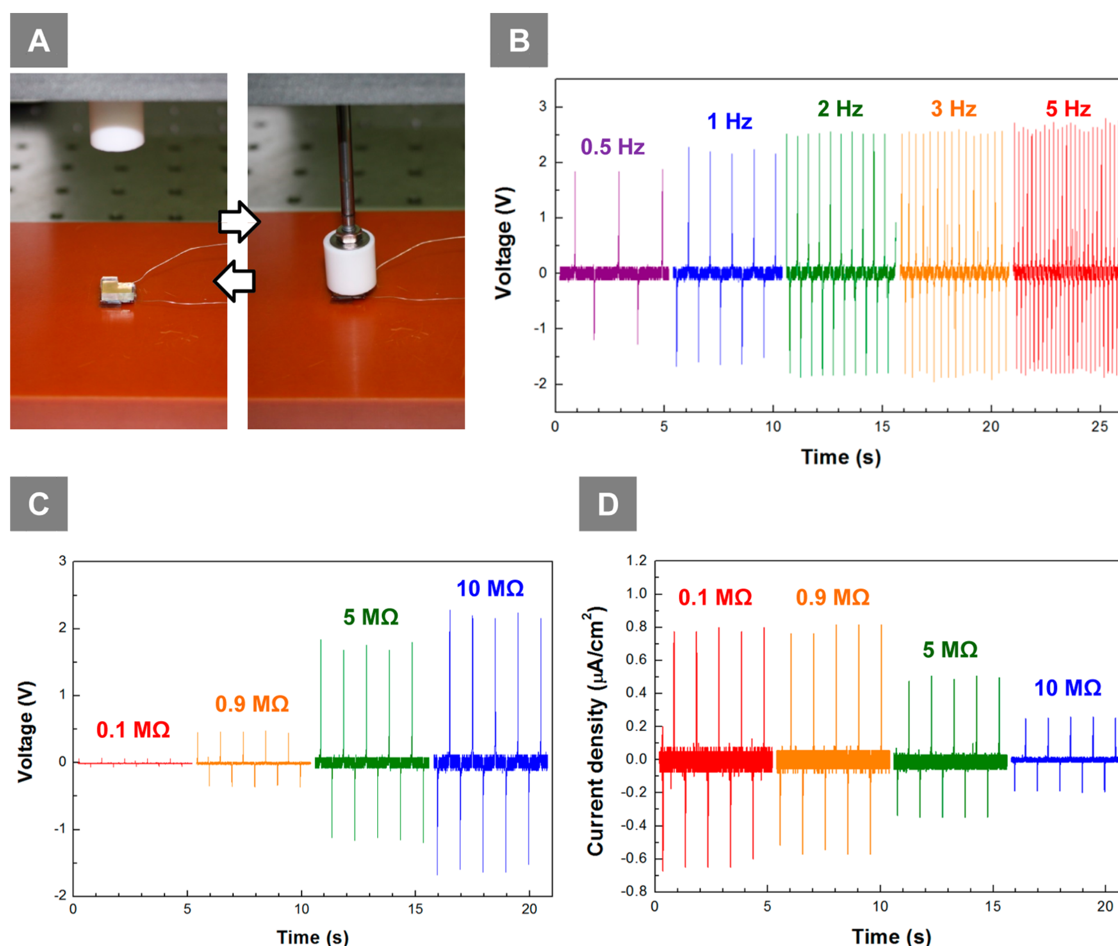

Figure 2. (A) Optical microscope images describing the experimental setup. The rigid cylinder repeatedly enables the push and release action of the PNG device. (B) Output voltage with various stress frequencies. Load resistance is 10 MΩ. (C) Output voltage with various load resistors. (D) Output current density with various load resistors.

serve as electrical insulation between the BTO layer and the top electrode. A margin of a sub-200 nm blocking layer is necessary between the BTO and the top Au electrode to function as the insulation of mobile carriers. Four important functions of the blocking layer are described in the previous literature.[19] Satisfaction of the design requirements is confirmed in the side-view SEM image in Figure 1F. An insulator margin of 100 nm between the layers was realized.

Iterative push and release actions were used to measure the piezoelectricity of the fabricated nanoshell PNG (Figure 2A).[20] The output voltage and current spectra are in good agreement with those of a conventional PNG's characteristics. A positive peak was observed at the moment the cylinder came into contact with the device, and a negative peak was noted at the moment the cylinder detached from the device.

Various cycling frequencies of the push and release process were applied (Figure 2B). Performances of PNGs are usually affected by the cycling frequency according to the previous reports.[21,22] Generated power increases the higher cycling frequency possibly because of the shorter potential rebalance time. A range of the frequency dependency differs by the type of PNG device, but 0.25 to 2.5 Hz is usually the sensitive range. In this case of the nanoshell PNG, the clear frequency dependency was observed in a range of 0.5 to 2 Hz. Output potential increases 43% when the forcing frequency increases from 0.5 to 5 Hz. To obtain higher instantaneous power, higher frequency excitation is desirable.

Performance of the PNG can also be affected by the load resistance. Optimum load resistance value depends on a kind of PNG used, hence characterization of the nanoshell PNG with various load resistors is important. A default value of load resistance is 10 MΩ, which is the load resistance of the oscilloscope for the measurement. When additional resistors are added, the oscilloscope resistor and additional resistor are connected in parallel. Three kinds of additional resistors with 10, 1, and 0.1 MΩ resistances were inserted for the experiment. Then the total equivalent load resistance became 5, 0.9, and 0.1 MΩ, respectively.

Because both internal resistance inside the PNG and load resistance outside the PNG simultaneously affect performances, both voltage–time and current–time

characteristics do not simply follow the linear relationship. Therefore, output power is not constant but varies by the load resistance. As the load resistance increased, generated voltage becomes larger and generated current becomes smaller. When the total equivalent load resistance was 0.1, 0.9, 5, and 10 MΩ, instantaneous voltage (*i.e.*, peak voltage) is 0.06, 0.46, 1.75, and 2.21 V, and instantaneous current density (*i.e.*, peak current density) is 0.79, 0.78, 0.49, and 0.25 $\mu A/cm^2$, respectively. Instantaneous power density also can be calculated by multiplying the instantaneous voltage and current density. The resulting power densities are 0.047, 0.363, 0.858, and 0.553 $\mu W/cm^2$ for the total resistance of 0.1, 0.9, 5, and 10 MΩ, respectively. The maximum power density was observed when the equivalent load resistance is in numbers of MΩ level; that is, it decreases when the load resistance is higher or lower than the optimal value. This bell-shaped relationship is well-matched with previously analyzed results discussed by Briscoe *et al.*[23]

A notable advantage of the top-down fabrication is the superior structural controllability. Structural parameters such as the specific shape of the structure, the size of the structure, and the location of the structure can be accurately controlled. For the optimization of the nanoshell PNG, comprehensive simulation analyses of the shell diameter and shell-to-shell space dependencies were performed. Conventional COMSOL software was used to extract the potential profiles.[24] A unit nanoshell block was modeled with a specific diameter and shell-to-shell space. Most structural parameters of the model were set to reflect actual device dimensions extracted from the fabricated device. Potential of the bottom part was grounded, and all sidewalls were assumed to be fixed and not deformed at all. After the structural setup, constant pressure was applied to the top of the device, and the potential profile can be extracted.

An important issue is how to extract the "measured voltage (V_{meas})" from the simulated potential profile. The simplest method is to use the maximum potential of the profile as a representative value; this is clearly inaccurate. The maximum potential is mainly observed on only a small part of the surface, and other parts have much smaller potentials than the maximum value. The most accurate method is to integrate all potentials of the profile and normalize the value with the device area. This method can be expressed by the following formula. $V(x,y)$ is the potential value at the specific location.

$$V_{meas} = \frac{\int_0^{S+D}\int_0^{S+D} V(x,y)\mathrm{d}x\mathrm{d}y}{(S+D)^2} \quad (1)$$

Despite the high accuracy, this approach is impractical because the method is too complex and requires serious labor and time consumption. Equation 1 can be further simplified without a significant sacrifice of the accuracy by adopting two assumptions. First, the potential of the nanoshell area is assumed to be constant with the value of the maximum potential (V_{max}). This assumption is plausible because the nanoshell has a symmetric circular shape, implying that the potentials of the top area in the nanoshell are virtually constant. Second, the potential outside of the nanoshell area is assumed to be zero. The bottom BTO film generates a small, not zero potential; however, the effects of those potentials are negligible because the values are much smaller compared to the potential of the nanoshell area. The simplified equation can be expressed as follows. Detailed simplification process is described in the Supporting Information.

$$\begin{aligned} V_{meas} &= \frac{V_{max}\{\pi(0.5D)^2 - \pi(0.5D-T)^2\}+0}{(S+D)^2} \\ &= \frac{V_{max}\pi T(D-T)}{(S+D)^2} \end{aligned} \quad (2)$$

where D, S, and T are the design parameters and V_{max} can be extracted from the profile, such that the simulated value of V_{meas} can be calculated. The simulated and the measured V_{meas} values are compared in terms of D and S (Figure 3) to provide a design guideline and to help establish design strategy. Both the D and S dependencies followed a bell shape. This bell-shaped relationship arises from the trade-off between V_{max} and the nanoshell density. A larger D and S always produce a larger V_{max} because forces from a wider area are concentrated on each nanoshell. In this case, however, the unit device area, that is, $(D + S)^2$, becomes larger. Consequently, only a small number of nanoshells exist in the total device area. Otherwise, when D and S are very small and the density of the nanoshell is therefore high, forces from only a small area are concentrated on each nanoshell. Thus, a small value of V_{max} is induced. Because both V_{max} and the device area increase for larger values of D and S, there should be an optimal point at which the largest V_{meas} value is produced. The optimal point in this simulation was observed when D is 6 μm and S is 3 μm (Figure 3A,B).

Devices with various values of D and S are measured and compared with the simulation results. We chose output voltage as a representative value for the comparison, but the current also follows a similar trend when high enough load resistance (10 MΩ) was used. Three devices for each condition are fabricated and measured to confirm the reproducibility. The experimental D dependency showed similar bell-shaped relationship with a D value of 6 μm (Figure 3C). Relatively larger error between the simulation and measurement occurred with a large D. This most likely occurred because the first assumption of the potential along the nanoshell has a constant value of V_{max} that

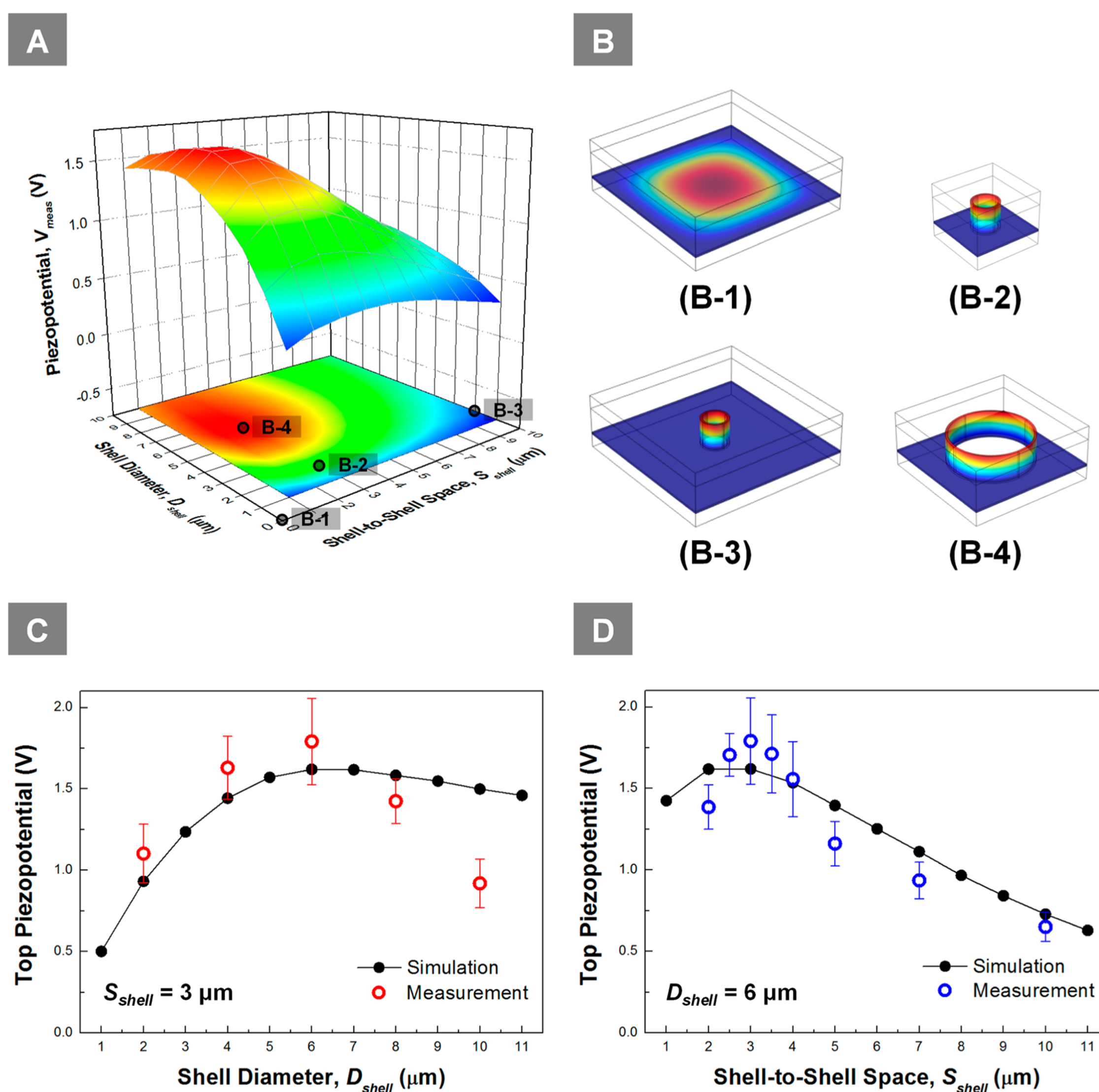

Figure 3. (A) Three-dimensional simulation graph of the predicted piezopotential with various shell diameters (D) and shell-to-shell spaces (S). The ranges of D and S are 1 to 10 μm with 1 μm steps. The value of the z-axis, V_{meas}, is calculated by simultaneously affecting maximum piezopotential and unit device area. (B) Simulation profiles of four specific unit blocks. B-1 represents a flat film morphology with D and S values of 0. The range of the color spectrum is 0 to 0.263 V. B-2 represents the unit nanoshell device with a D value of 2 μm and an S value of 3 μm. The range of the color spectrum is 0 to 12.6 V. B-3 represents the unit nanoshell device with a D value of 2 μm and an S value of 10 μm. The range of the color spectrum is 0 to 34.0 V. B-4 represents the unit nanoshell device with a D value of 6 μm and S value of 3 μm. The range of the color spectrum is 0 to 22.4 V. (C) Simulation and measurement results of the D dependency when S is fixed at 3 μm. Simulated curves are linearly fitted to produce the best match with the measured results. Error bars represent the standard deviations of a total of 30 peaks from three devices. (D) Simulation and measurement results of the S dependency when D is fixed at 6 μm. Simulated curves are linearly fitted to produce the best match with the measured results. Error bars represent the standard deviations of a total of 30 peaks from three devices.

would not be feasible for a large D. The potential profile along the large nanoshell was not as uniform as that with a small nanoshell. The differences between the actual and assumed potential profile may cause a slight discrepancy. The experimental S dependency also showed a bell-shaped relationship without significant differences. Both the simulation and measured data reveal that the optimal range of S of the nanoshell PNG is between 2 and 4 μm.

To verify the measured spectrum stemming from the piezoelectricity, a linear superposition test was conducted. Two nanoshell PNGs were serially connected with Al wires (Figure 4). One device generated a 2 V peak potential, and the other device generated a 3 V peak potential for the same pressure. During the short period of action, the PNGs can be modeled as a voltage source with serially connected stack capacitor, loss resistor, and leakage resistor.[25] When the two devices were serially connected and the same pressures were applied to both of the devices, 5 V peaks were observed because the two sources were summed. The bottom peaks, caused during the

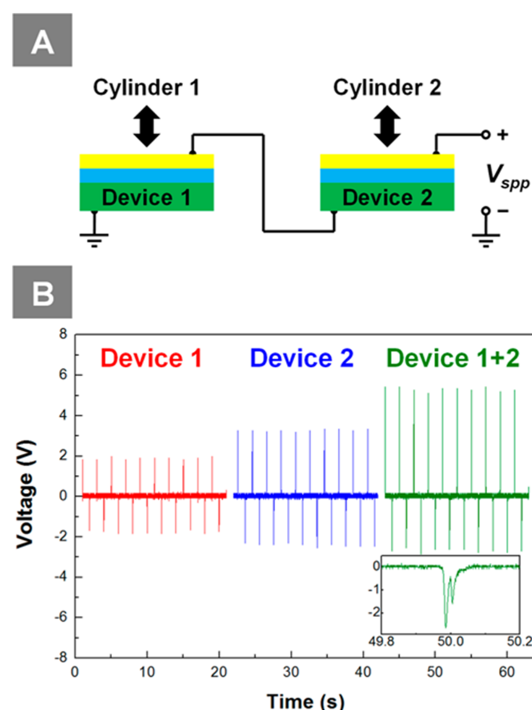

Figure 4. (A) Schematic describing the wiring setup of the linear superposition test. Two devices are serially connected, and two cylinders simultaneously experience push and release stress in both devices. (B) Results of the superposition test. The output piezopotentials of individual devices are summed after the serial connection. The inset describes the double peak feature which is caused by the asynchronicity of the release timing.

release process, presented double peaks because two cylinder movements were not perfectly synchronized. The double peak shape also confirmed that the superposition phenomenon is evidence that assures piezoelectricity. Consequently, the result of the superposition test indicates that the measured results were caused by the actual piezopotential and not by any environmental effect.[7,26,27]

CONCLUSION

In summary, a PNG with a well-ordered nanoshell array structure was proposed and analyzed. The nanoshell array was fabricated using a top-down silicon nanofabrication process instead of the conventional bottom-up growth process. A spacer lithography technique was applied to form a wafer-scale, well-ordered BTO nanoshell array with nanoscale thickness, which cannot be done with conventional photolithography. Using the excellent structural controllability of the top-down fabrication process, the geometrical dependency of the nanoshell array could be analyzed. Both the simulated and the measured piezopotential showed a bell-shaped relationship of the shell diameter and the shell-to-shell space. This result implies that the nanoshell PNG should be deliberately designed with a proper range, rather than be created without a design strategy. Given this finding, the well-ordered structure as presented here is advantageous for the accurate geometrical optimization of PNGs. Additionally, the entire process is CMOS-compatible, which implies that such a device can be profitable when used in chip-based integrated system applications.

METHODS

The fabrication procedure of the nanoshell PNG is composed of two parts: the skeleton nanoshell fabrication part and the functional layer deposition part. Detailed schematics of each fabrication step are shown in the Supporting Information (Figure S1). Fabrication begins with an 8 in. p-type silicon wafer. Thermal oxidation is applied to form a 200 nm layer of silicon dioxide (SiO_2). Then, the microhole array is patterned onto the substrate by means of photolithography. The patterned area is then dry-etched to a depth of 10 μm. On the microhole array, a 50 nm silicon nitride (Si_3N_4) layer is deposited by a low-pressure chemical vapor deposition (LPCVD) process. The Si_3N_4 layer conformally covers the microhole array due to the extremely high step coverage of the LPCVD process. Subsequently, the top layer of the Si_3N_4 is selectively removed using a chemical–mechanical polishing (CMP) process. During the CMP process, the SiO_2 layer serves as an etch-stop layer protecting the underneath microhole array. SiO_2 and Si substrate are then etched to a depth of 2 μm to form the skeleton of the Si_3N_4 nanoshell array.

On the skeleton nanoshell array, a 200 nm barium titanate ($BaTiO_3$, simply BTO) film is deposited using RF sputtering. The physical vapor deposition (PVD)-based sputtering technique used in this work is different from the widely adopted high-pressure sputtering-based epitaxial growth process.[28] BTO is a widely adopted piezoelectric material that has the advantages of a relatively high piezoelectric coefficient and a lead-free composition. A crystallization process is subsequently conducted on the BTO nanoshell array under O_2 ambient conditions at 700 °C for 20 min. Characterization of the BTO film before and after the crystallization process is discussed in the Supporting Information. The next step of the fabrication process is the blocking layer deposition. In this device, HKT-501 polymer film is spin-coated onto the BTO nanoshell array at 2000 rpm. The target thickness is slightly less than 2 μm, but the top of the nanoshell is also covered with the polymer due to the high viscosity. Onto the polymer layer, a Cr adhesion layer and a Au electrode layer are sequentially deposited to serve as the top electrode.

To finalize the device fabrication, Al wires are held in contact with both the top and bottom electrodes by means of silver paste. To align the dipole direction of the BTO layer, a poling process was performed with an electric field of 50 kV/cm at 150 °C for 10 h. A statistical analysis of the poling dependency is included in the Supporting Information. Here, the output piezopotential was significantly enhanced after the poling process.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Details of the fabrication process and statistical analyses pertaining to the poling dependency are provided in the Supporting Information. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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